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Design and analysis of RCA in Subthreshold Logic Circuits Using AFE

[1]MAHALAKSHMI M, [2]P.THIRUVALAR SELVAN

PG Student, VLSI Design, Department of ECE, TRPEC, Trichy

Abstract: **The present scenario of the circuit subthreshold CMOS logic circuits is becoming increasingly popular energy- constrained applications where high performance is not required. Minimum energy consumption of digital logic circuits can be obtained by operating in the subthreshold regime. However, in this regime process variations can result in up to order of magnitude variations in I_{ON} / I_{OFF} ratios leading to timing errors, which can have a destructive effect on the functionality of the subthreshold circuits. These timing errors become more frequent in scaled technology nodes where process variations are highly prevalent. Therefore, mechanisms to mitigate these timing errors while minimizing the energy consumption are required. In this proposed work, Low power subthreshold logic circuits using adaptive feedback equalizer circuit is designed. The adaptive equalizer technique is used with a sequential digital logic to mitigate the process variation effects and reduce the dominant leakage energy components in the subthreshold digital logic circuits. The performance of the proper circuit is evaluated for different input voltages, other work for 4 bit Ripple Carry Adder in designed using to the logic gate size and power is discussed in the simulation is successfully in verified with the help of Microwind and Dsch tool.**

Keywords: **Adaptive Feedback equalizer, Low power subthreshold, variable threshold inverter, Ripple Carry Adder.**

I. INTRODUCTION

The subthreshold digital CMOS logic circuits are becoming increasingly popular in energy-constrained applications where high performance is not required. The main idea here is that scaling down the supply voltage can significantly reduce the dynamic energy consumed by digital circuits. Scaling down the supply voltage also lower down the current due to a reduction in the drain-induced barrier lowering (DIBL) effect. Moreover, the supply voltage is scaled below the threshold voltage of the transistors, the propagation delay of the logic gates increases, which in turn increases the leakage energy of the transistors. These two opposite trends in the leakage and the dynamic energy components lead to a minimum energy supply voltage that occurs below the threshold voltage of the transistors for digital logic circuits [1]. However, digital logic circuits operating in the subthreshold region suffer from process variations that directly affect the threshold voltage (V_T). This, in turn, has a significant impact on the drive current due to the relationship between the drive current and the threshold voltage of the transistors is the sub threshold regime. Moreover, subthreshold digital circuits suffer from the degraded I_{ON} / I_{OFF} ratios [2] resulting in a failure in providing rail-to-rail output swings when restricted by aggressive timing constraints. These degraded I_{ON} / I_{OFF} ratios and process-related variations make subthreshold circuits highly susceptible to timing errors that can further lead to complete system failures. Since the standard deviation of V_T varies inversely with the square root of the channel area [3], one approach to overcome the process variation is to upsize the transistors [2]. Alternately, one can increase the logic path depth to leverage the statistical averaging of the delay across gates [4] to overcome process variations. These approaches, however, increase the transistor parasitics, which in turn increases the energy consumption. In this paper, we first propose the use of a feedback equalizer circuit for lowering the energy consumption of digital logic operating in the subthreshold region while achieving robustness equivalent to that provided by [2]. Here, the feedback equalizer circuit (placed just before the flip-flop) adjusts the switching threshold of its inverter based on the output of the flip-flop in the previous cycle to reduce the charging/discharging time of the flip-flop's input capacitance. Moreover, the smaller input capacitance of the feedback equalizer reduces the switching time of the last gate in the combinational logic block. Overall, this reduces the total delay of the sequential logic, which makes it more robust to timing errors and allows aggressive clocking to reduce the dominant leakage energy. In addition to reducing

energy consumption, we also demonstrate how the tuning capability of the equalizer can be used to enable extra charging/discharging paths for the flip-flop input capacitance after fabrication to mitigate timing errors resulting from worse than expected process variations in the subthreshold digital logic. In general, our approach of using feedback equalizer to lower energy consumption and improve robustness is independent of the methodology used for designing a combinational logic block operating in the subthreshold regime. The main contributions of this paper are as follows.

1) We propose using an adaptive feedback equalizer circuit in the designing subthreshold digital logic circuits. This adaptive feedback equalizer circuit can reduce energy consumption and improve the performance of the subthreshold digital logic circuits.

2) We present detailed analytical models (AMs) for performance and energy of the adaptive feedback equalizer circuit. The models can be easily used in combination with the existing performance and energy model for subthreshold logic circuits to generate designs that meet energy and performance constrains.

II. ADAPTIVE EQUALIZED FLIP-FLOPVERSUS CONVENTIONAL FLIP-FLOP

In this section, we first explain the use of the adaptive feedback equalizer circuit and the design of an Adaptive equalized flip-flop (E-flip-flop) and then provide a detailed comparison of the E-flip-flop with the conventional flip-flop in terms of area, setup time, and performance. The proposed there is the use of a variable threshold inverter [5] as an adaptive feedback equalizer along with the classic master-slave positive-edge-triggered flip-flop [6] (Fig. 2) to design an adaptive E-flip-flop. This adaptive feedback equalizer circuit consists of two feed forward transistors (M1 and M2 in Fig. 1) and four control transistors (M3 and M4 for feedback path 1

Table I: Propagation Delay

Min.supply Voltage (mV)	Delay NE-logic (ns)	Delay E-logic (ns)	Delay Buffer NE-logic (ns)
950	681.5	881	681.2
900	681.2	880.8	681.1
850	681	880.4	680.5
800	680.4	880	680
750	680	879	679
650	678	877	679
620	677	876	675
550	672	872	665

Table II: Leakage Power

Min.supply Voltage (mV)	Leakage Power E-logic(µW)	Leakage Power NE-logic (µW)	Leakage Power Buffer NE(µW
950	6.1	6.6	4.8
900	4.9	6.0	4.3
850	4.5	4.2	4.9
800	3.7	4.0	4.9
750	3.3	3.7	4.7
650	2.6	3.0	4.5
620	2.4	2.8	4.2
550	2.2	2.0	2.9

TABLE III: Power Delay Product

Min supply voltage (mV)	PDP NE-logic (nW)	PDP E-logic (nW)	PDP buffer NE-logic (nW)
950	4157.2	5814.6	3269.7
900	3338	5284.4	2928.7
850	3064.5	3697.6	3332.6
800	2516.4	3520	3334.4
750	2244	3252.3	3191.3
650	1762.8	2631	3055.5
620	1624.8	2452.8	2835
550	1478.4	1744.2	1928.5

The adaptive E-flip-flop has eight more transistors than the conventional master–slave flip-flop [29]. Compared with a classic master–slave flip-flop with 22 transistors [seven inverters and four transmission gates (TGs)], the area overhead of the adaptive E-flip-flop is 36%.The area overhead of the control latch with ten transistors (three inverters and two TGs) 45%. This area overhead gets amortized across the entire sequential logic block.

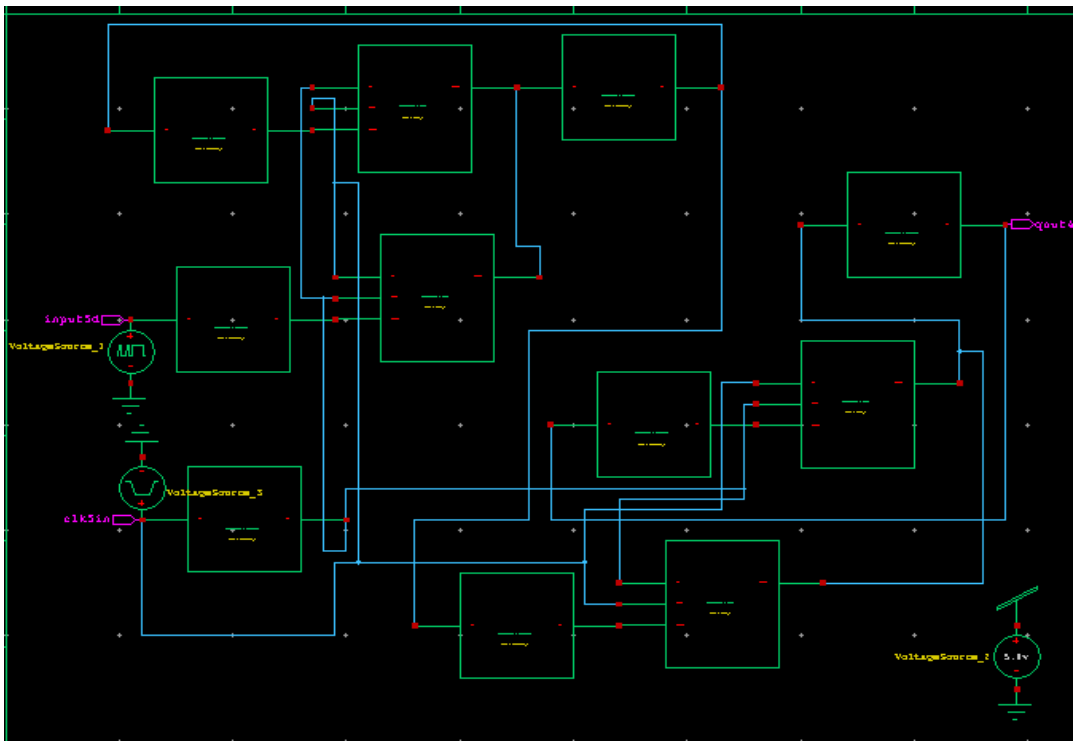

Fig 1: Circuit diagram of classic master-slave positive edge- triggered flip-flop

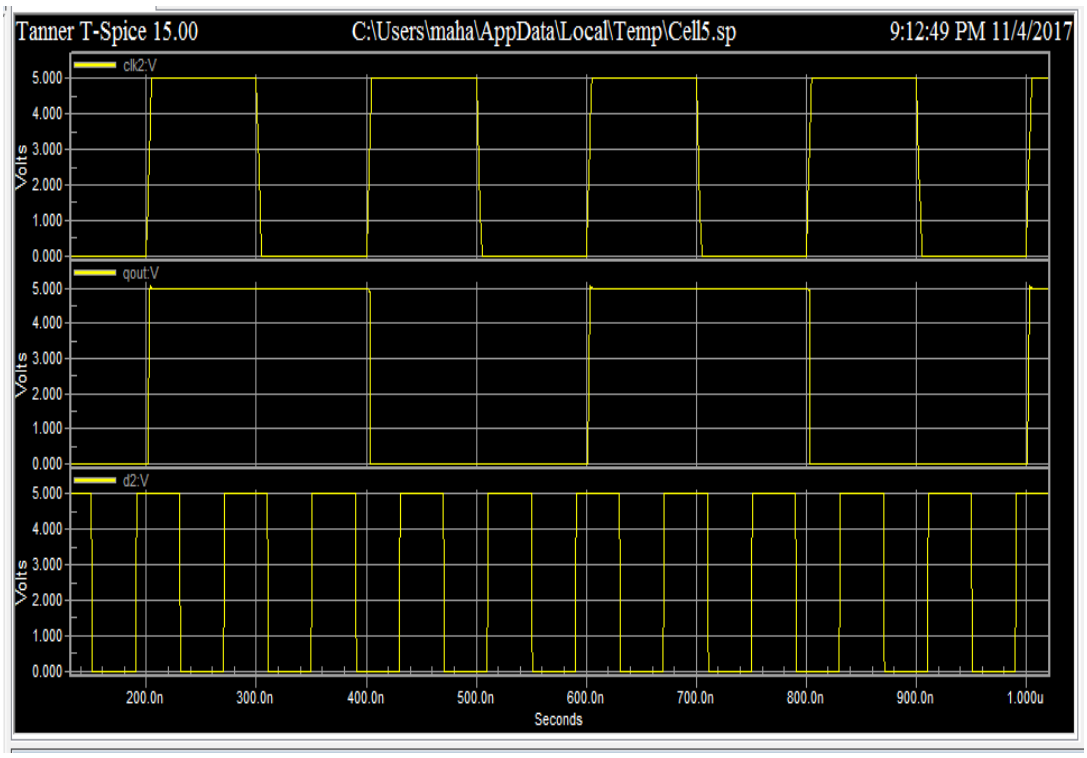

Fig 2: Simulation result of classic master-slave positive-edge-triggered flip-flop

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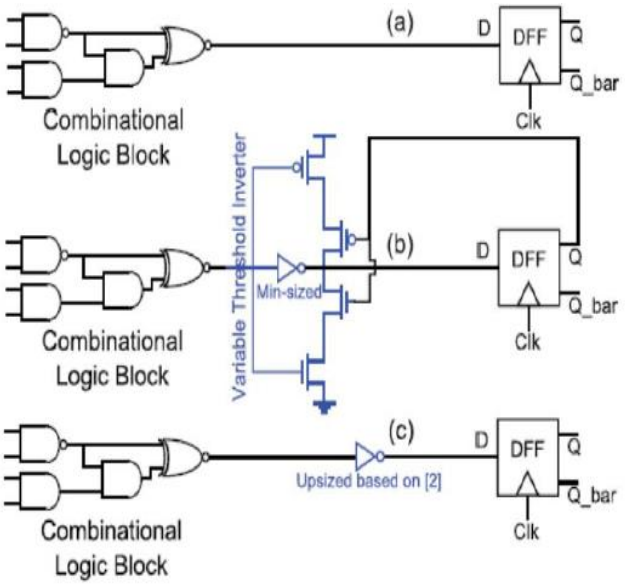

Fig 3: Block diagram of (a) original nonequalized design, (b) equalized design with one feedback path ON, and (c) buffer-inserted nonequalized design.

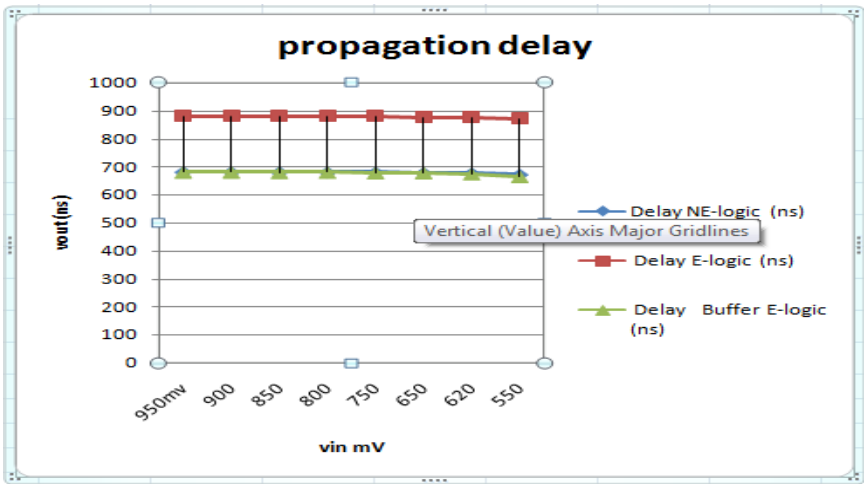

Fig 4: Propagation Delay

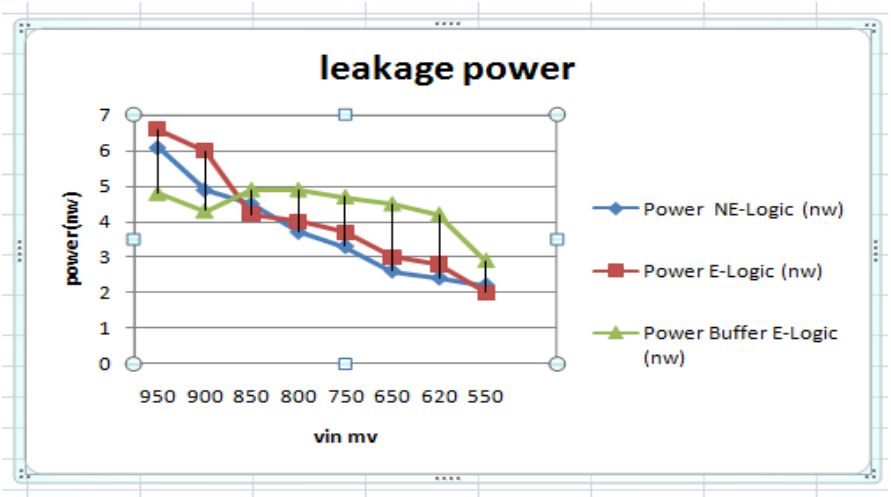

Fig 5: Leakage Power

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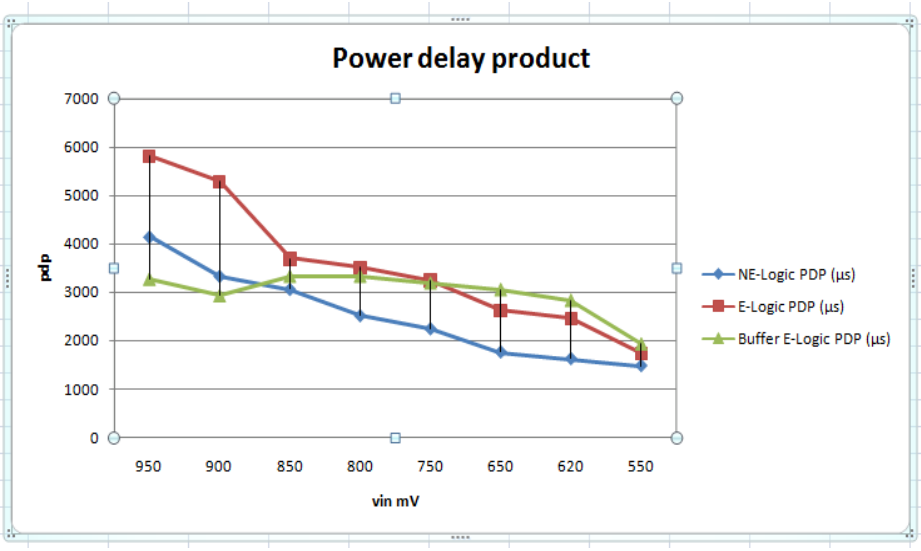

Fig 6: Power Delay Product

III. 4 BIT RIPPLE CARRY ADDER

Logical circuit with multiple full adders can be used for adding N-bit each full adder input a Cin, which is the Cout of the previous adder. Such kind of adder is known as Ripple Carry Adder. RCA in digital electronics is that circuit which produces the arithmetic sum of two binary numbers which can be constructed with full adders connected in cascaded with the carry output from each full adder connected to the carry input of the next full adder in the chain as shown fig 1.8 From which it can be noticed that bits a0and b0 in the fig represent Carry Adder, each carry bit “ripples” to the next full adder. the least significant bits of the number which is to be added and sum in form output represented by the bits (s0-s3). A design of RCA based on NAND gate and is a symbol is done simply.

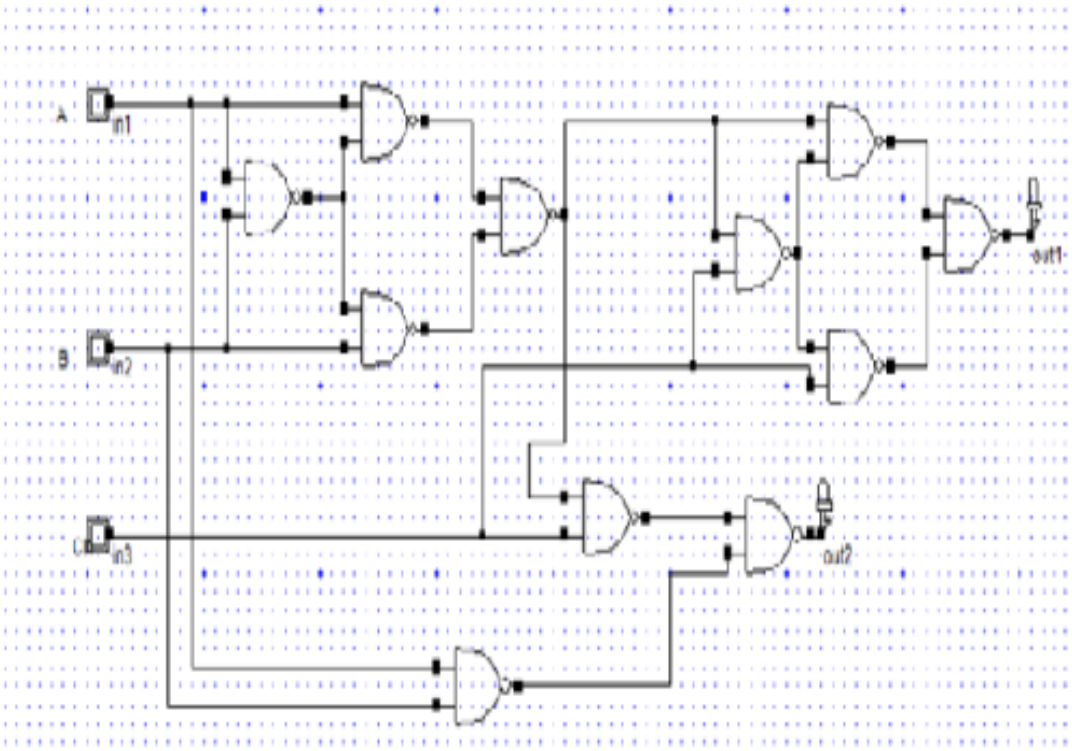

Fig 7: RCA in NAND gate Circuit diagram

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TABLE IV: RCA in Truth table

INPUT		INPUT	OUTPUT	OUTPUT
A	B	C_{in}	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

IV. RESULT AND DISCUSSION

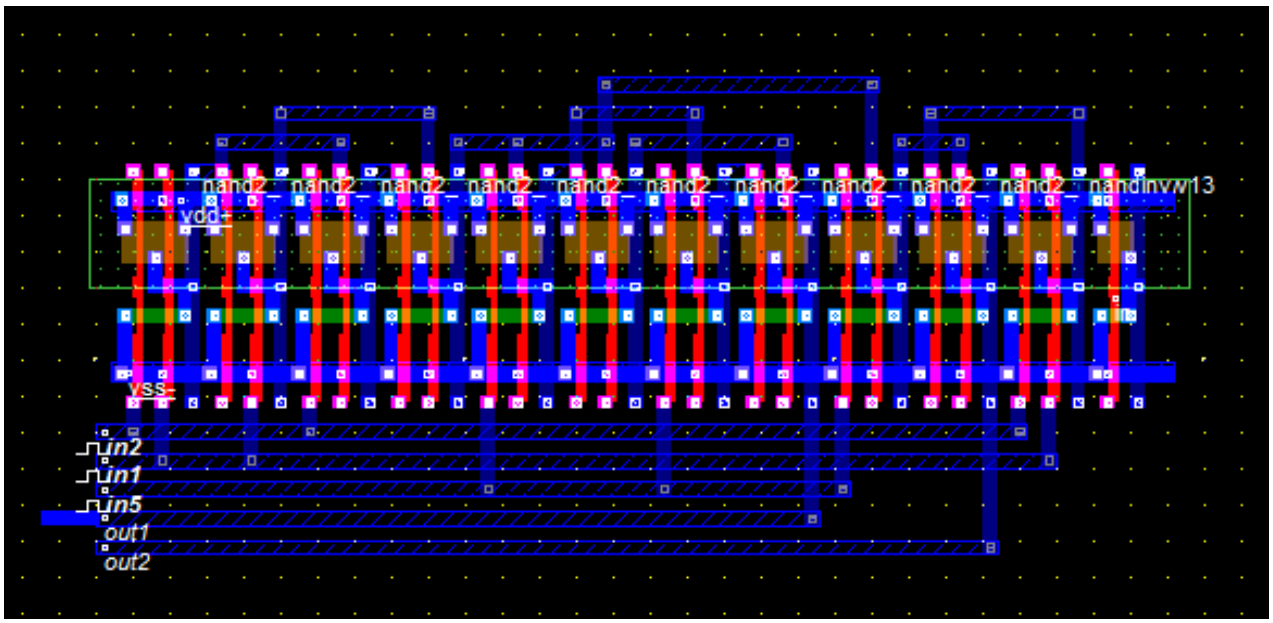

Fig 8: Layout in RCA

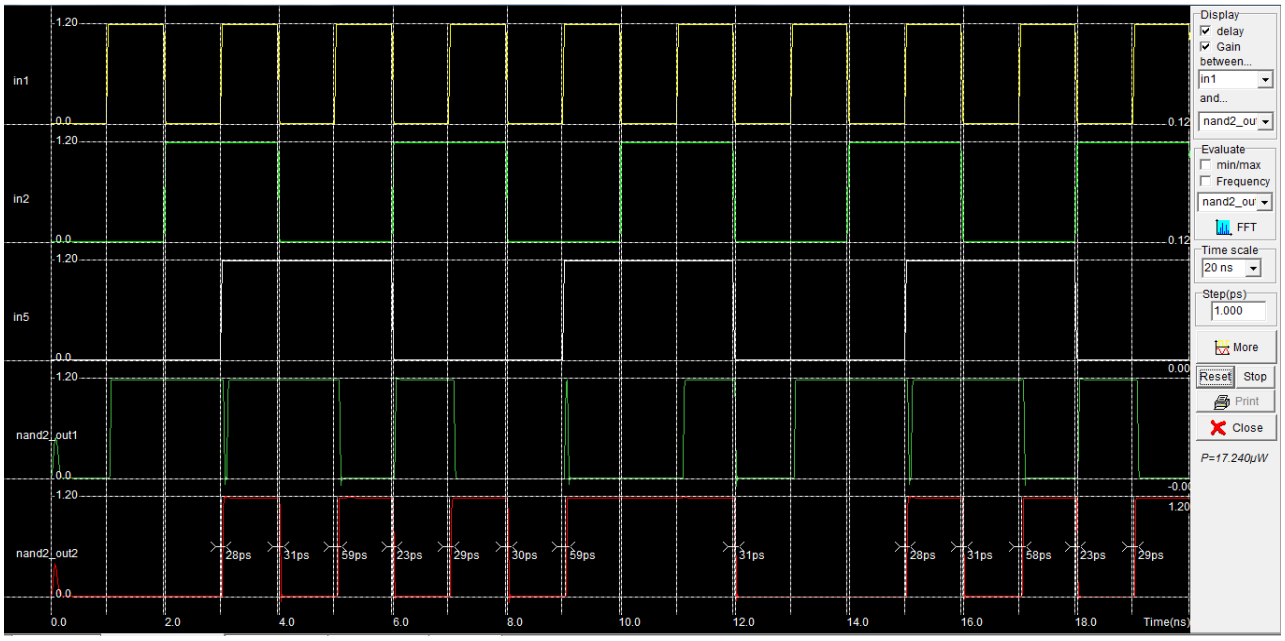

Fig 9: Analog simulation result in RCA

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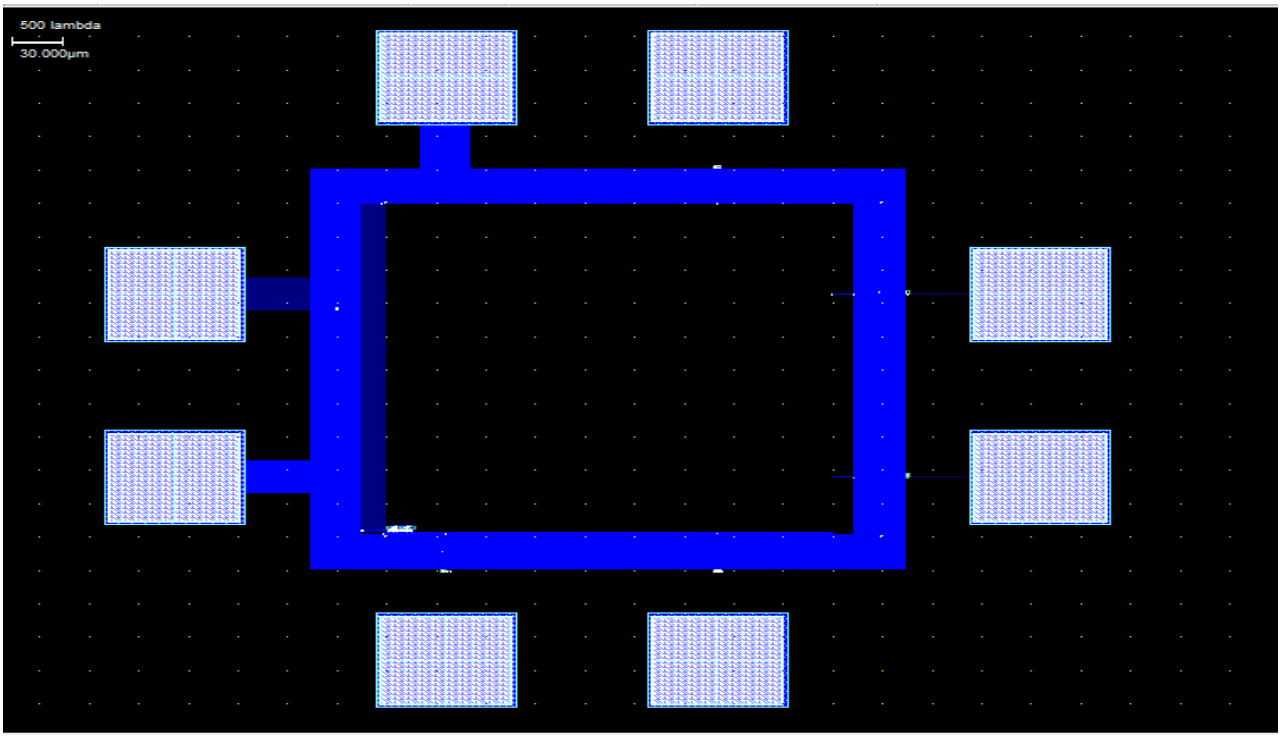

Fig 10: FPGA Output

V. POWER ANALYSIS

The leakage power, propagation delay and the product of power and delay are shown in Table (I,II, III) When the input voltage is reduced. The propagation delay of an equalized flip flop is reduced from 681.5µs to 672µs. The proposed low power subthreshold logic circuits are used for Adaptive Feedback Equalizer circuit and 4 bit RCA can be designed. The RCA can be used for the logic circuit that calculates the power delay and reduces the power consumption.

VI. CONCLUSION

The proposed adaptive feedback equalizer circuit to reduce the normalized variation of propagation delay along the critical path and the dominant leakage power of the digital CMOS logic operating in the subthreshold regime. Adjusting the circuit switching threshold of the gates before the flip-flop based on the gate output in the previous cycle, the adaptive feedback equalizer circuit enables a faster switching of the gate outputs and provides the opportunity to reduce the leakage power of digital logic in weak inversion region. The adaptive feedback equalization circuit to the propagation delay of an equalized flip-flop from 681.ns to 672ns, the power consumption of Equalized flip-flop from 6.6µW to 2.0µW and Power Delay product reduced in different input voltage. The NAND gate used for the 4 bit Ripple Carry Adder designed using logic gate size power is discussed in the simulation is successfully verified.

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